Structural, Optical, and Electrical Properties of Silicon Nanowires for Solar Cells

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***Abstract*-We investigated Si nanowires (SiNWs) fabricated by wet etching and chemical vapor deposition (CVD), and core-shell structures, formed by depositing silicon layers around the SiNWs, with respect to their crystallinity, the doping level, and the influence of surface passivation on carrier lifetime. The effects expected to be critical to improve the performance of nanowire-based solar cells are discussed.**

BACKGROUND

Nanowire-based photovoltaic structures are currently of great interest due to their potential to reduce manufacturing costs while allowing to keep good efficiencies and device lifetimes. In particular, several SiNW based solar cell concepts have been demonstrated, but the efficiencies are mostly below 2% at this stage [1-4].

Further improvements of device performance are expected to be possible by increasing material quality e.g. the crystallinity of the shell layer in a core-shell p-n junction cell. Another option could be to minimize or avoid the presence of gold as a catalyst in the vapor-liquid-solid (VLS) growth process. Furthermore, improving the surface passivation of the SiNWs could reduce carrier recombination at surface traps.

Here, we describe the fabrication of SiNWs to be used in a thin film solar cell. The p-n junction is realized in a core-shell configuration by deposition of an amorphous hydrogenated Si (*a*-Si:H) shell with opposite doping than the wire itself, and subsequent crystallization of the shell by annealing.

RESULTS

Au nanoparticles (AuNP) of 15-150 nm diameter immobilized on Si or glass substrates were used to produce diameter controlled SiNWs in a CVD reactor. The wires were grown by the VLS method and doped using PH_3 and B_2H_6. For comparison, SiNW arrays were made by an etching method using a solution of silver nitrate and hydrofluoric acid [5]. The etched wires do not suffer from gold incorporation into the SiNWs, but the diameters are more difficult to control and they show a high surface roughness.

To evaluate the effective minority carrier lifetime of undoped SiNWs realized by the two different methods, contactless quasi-steady-state photoconductance (QSSPC) measurements were performed [6]. In this set-up, the change in conductance of the samples during exposure to a slowly decaying flashlight is measured and allows for the calculation of the effective carrier lifetime, averaged over the structure that is tested, as function of the excess carrier density. Table 1 summarizes results of measurements on as-grown structures, after a brief HF dip, and after thin *a*-Si:H film deposition [7].

For reference, lifetime measurements were also performed on a bare Si wafer without SiNWs. These results show that to some extent, HF passivates the surface already, although the intrinsic *a*-Si:H passivation is by far more effective. Next, the table also shows the case of SiNWs synthesized by metal-catalysts. Here, it can be seen that the passivation results after HF dip and intrinsic *a*-Si:H deposition basically do not change, compared to the as-grown case. This contrasts with the case of chemically etched SiNWs, where a clear improvement in surface passivation can be observed.

Due to the fact that for all structures tested, the passivation treatments were identical, the essentially not-effective passivation results in the case of SiNWs grown by a Au-catalyzed VLS process can most likely be attributed to poisoning of the SiNWs with gold atoms and perhaps poisoning of wafer-surfaces as well.

It is worth noting that the carrier lifetimes of the CVD-grown SiNWs appear to be higher than typical values reported in the literature [1,8]. To a large extent, this should be due to the QSSPC measurement method employed, where the measured lifetimes are rather an integrated value over the entire test-structure. Nevertheless, as the *effective* carrier-lifetime of test-structures is typically dominated by the electronically inferior component, these measurements most likely give at least an indirect indication of the effective carrier lifetimes in our SiNWs.

Electron beam-induced current (EBIC) imaging [9] was used to demonstrate the successful activation of the dopants in the wires, and current-voltage (*I-V*) measurements show the rectifying behavior of the p-n junctions. The dark spot seen in the right inset of Fig. 1 indicates an EBIC flowing from the substrate (n-type) to the Pt-Ir tip through the boron-doped SiNW, and the junction is located at the nanowire-substrate interface. The *I-V* curve shown in Fig. 1 is rectifying with the forward direction from the Pt-Ir tip to the nanowire. For a

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Acknowledgment: This work was in part supported by the European Commission (ROD_SOL, FP7-NMP-227497).

978-1-4244-3544-9/10/$25.00 ©2010 IEEE

TABLE I Minority carrier lifetime measured for silicon wafers with differently prepared SiNWs in dependence on the surface passivation quality.

Surface conditions	Effective carrier lifetime of test-structures (µs, at $\Delta n = 10^{14}$ cm^{-3})				
	Si wafer 28 Ωcm	Si wafer with SiNWs 2 nm Au film	Si wafer with SiNWs 30 nm AuNP	Si wafer with SiNWs 60 nm AuNP	Si wafer with SiNWs chemically etched
native oxide	1.0	0.9	1.0	1.0	1.3
HF dip	14.5	0.9	1.5	1.2	17
50 nm intrinsic a-Si 200°C, 30 min	1041	0.7	1.5	0.8	36

phosphorus-doped SiNW grown on a p-type silicon substrate a bright spot indicates an EBIC flowing from the Pt-Ir tip through the wire to the substrate with the junction located at the nanowire-substrate interface, and a rectifying *I-V* curve with the reverse direction from the Pt-Ir tip to the nanowire (not shown).

The crystallization behavior of the *a*-Si shell on top of the SiNW core after removing gold and the native oxide was studied by transmission electron microscopy (TEM). Clean, oxide-free surface conditions are essential for achieving epitaxial growth. At this stage annealing yields polycrystalline shells as shown in Fig. 2. Furthermore, the crystallization rates vary between the samples probably due to impurity effects.

Optical absorption data of SiNWs with different diameters on glass substrates were obtained by measuring the transmission and reflection spectra using a UV-vis/NIR spectrometer equipped with an integrating sphere. Fig. 3 shows the absorption of 15 and 150 nm diameter SiNWs compared to a Si wafer.

SiNWs transferred on an oxidized silicon substrate were individually contacted using electron-beam lithography and the resistivity was measured by the four-probe method. The I-V characteristics of the SiNW solar cells were measured in the dark and under AM 1.5 illumination conditions and will be presented at the conference.

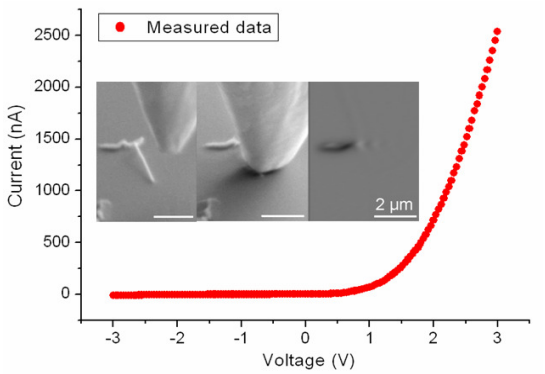

Fig. 1. Current-voltage characteristics measured on a boron-doped nanowire grown on a n-type substrate as shown in the left inset. Center inset is a secondary electron (SE) image of the tip in contact with the nanowire. Right inset is an EBIC image of the p-n junction located at the nanowire-substrate interface.

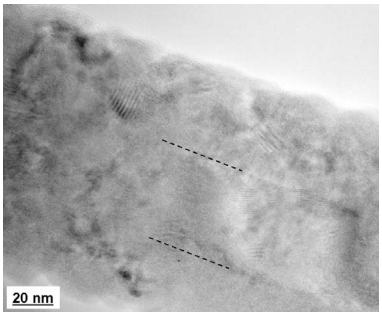

Fig. 2. TEM image showing the single crystalline CVD-grown SiNW core (dashed line as a guide to the eye) and polycrystalline Si shell after annealing.

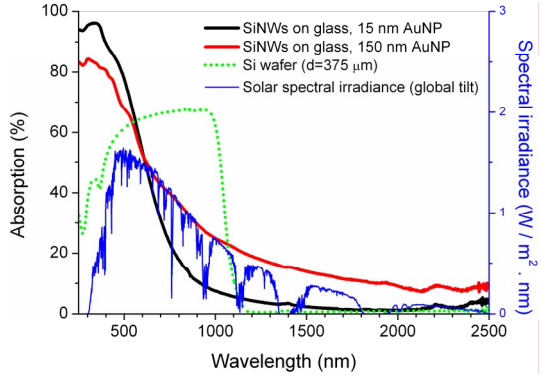

Fig. 3. Optical absorption of SiNWs with different diameters on glass substrate compared to the absorption of a 375 µm thick Si wafer. Furthermore, the terrestrial solar spectral irradiance is given.

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